

# Ashay Rane

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## Contact Information

GDC 5.518F, 1 University Station,  
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<https://ashay.rane.info>

## Research Interests

Secure Systems, Compilers, Computer Architecture, and Program Verification.

## Education

- ▶ **PhD in Computer Science** GPA: 3.54  
The University of Texas at Austin, Austin, Texas. *Aug 2012 – May 2019*
- ▶ **Master of Science in Computer Science** GPA: 4.0  
Arizona State University, Tempe, Arizona. *Aug 2007 – Nov 2009*
- ▶ **Bachelor of Engineering in Computer Engineering** Aggregate: 72.43%  
Mumbai University, Mumbai, India. *Jun 2003 – Jul 2006*

## Honors and Awards

- ▶ **Distinguished Paper Award**, at the USENIX Security Symposium (2017).
- ▶ **Brumley Senior Next-Generation Fellow**, Robert Strauss Center for International Security and Law, The University of Texas at Austin, 2015 and 2016.
- ▶ **Best paper nominee**, at the International Conference on Parallel Architectures and Compilation Techniques (2012).

## Work Experience

- ▶ **Compiler Engineer, Groq** *Aug 2019 – present*  
I work on the compiler and programming tools for Groq's Tensor Streaming Processor.
- ▶ **Graduate Research Assistant, Computer Science, UT Austin** *Sep 2012 – May 2019*  
I did research in compiler and microarchitectural defenses against side-channel attacks.
- ▶ **Intern, Galois, Portland, Oregon** *May 2018 – Aug 2018*  
I researched and developed tools for identifying side-channel information leakage in Verilog code.
- ▶ **Research Educator (Instructor), UT Austin** *Jan 2015 – Dec 2016*  
I taught a freshman course on computer security [[cs.utexas.edu/users/fri-security](https://cs.utexas.edu/users/fri-security)], where the objective was to teach research skills to freshman students. Students critiqued research papers, discussed extensions, and implemented research projects.
- ▶ **Intern, Microsoft Research, Redmond, Washington** *May 2016 – Aug 2016*  
As part of the Project Everest group [<https://project-everest.github.io>], I designed and implemented a verified digital side-channel leakage analyzer using the Dafny verifier.
- ▶ **Intern, Google, California** *May 2013 – Aug 2013*  
I analyzed and optimized the performance of Cloud SQL on Google's infrastructure.

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## Work Experience (*continued*)

- ▶ **Research Associate, Texas Advanced Computing Center** *Dec 2010 – Aug 2012*  
I researched and developed tools for performance diagnosis of data center applications.
- ▶ **Performance Engineer, Salesforce.com, California** *Feb 2010 – Nov 2010*  
I improved performance of the Apex and VisualForce language runtimes, and designed tools for automation of performance tuning.
- ▶ **Graduate Research Assistant, Arizona State University** *Jan 2008 – Nov 2009*  
I studied hybrid (or mixed-mode) programming using MPI and OpenMP.
- ▶ **Research Intern, SAP Research, California** *May 2008 – Aug 2008*  
I designed and implemented a parallel debugger for SAP's threading library.
- ▶ **Graduate Research Assistant, Arizona State University** *Aug 2007 – Dec 2007*  
I designed and implemented a sourceforge-like web portal for the OpenABM consortium.

## Publications

- ▶ B. Bond, C. Hawblitzel, M. Kapritsos, K. Leino, J. Lorch, B. Parno, **A. Rane**, S. Setty, L. Thompson, “*Vale: Verifying High-Performance Cryptographic Assembly Code*”, USENIX Security, Symposium, August 2017. **Distinguished Paper Award**
- ▶ **A. Rane**, C. Lin, M. Tiwari, “*Secure, Precise, and Fast Floating-Point Operations on x86 Processors*”, USENIX Security Symposium, August 2016.
- ▶ **A. Rane**, C. Lin, M. Tiwari, “*Raccoon: Closing Digital Side-Channels through Obfuscated Execution*”, USENIX Security Symposium, August 2015.
- ▶ **A. Rane**, R. Krishnaiyer, C. Newburn, J. Browne, L. Fialho, Z. Matveev, “*Unification of Static and Dynamic Analyses to Enable Vectorization*”, International Workshop on Languages and Compilers for Parallel Computing (LCPC), September 2014.
- ▶ **A. Rane**, J. Browne, “*Enhancing performance optimization of multicore/multichip nodes with data structure metrics*”, ACM Transactions on Parallel Computing, May 2014.
- ▶ **A. Rane**, J. Browne, “*Enhancing performance optimization of multicore chips and multichip nodes with data structure metrics*”, Parallel Architectures and Compilation Techniques (PACT), September 2012 - Nominated as one of 3 best papers of the conference.
- ▶ **A. Rane**, J. Browne, L. Koesterke, “*A Systematic Process for Efficient Execution on Intel's Heterogeneous Computation Nodes*”, Extreme Science and Discovery Environment (XSEDE), July 2012.
- ▶ **A. Rane**, J. Browne, L. Koesterke, “*PerfExpert and MACPO: Which code segments should (not) be ported to MIC?*”, TACC-Intel Highly Parallel Computing Symposium, April 2012.

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## Publications *(continued)*

- ▶ **A. Rane**, S. Sardeshpande, J. Browne, “*Determining code segments that can benefit from execution on GPUs.*”, Supercomputing Conference (SC) 2011, November 2011.
- ▶ **A. Rane**, J. Browne, “*Performance Optimization of Data Structures using Memory Access Characterization.*”, IEEE International Conference on Cluster Computing (CLUSTER), 2011, September 2011.
- ▶ O. A. Sopeju, M. Burtscher, **A. Rane**, and J. Browne, “*AutoSCOPE: Automatic Suggestions for Code Optimizations Using PerfExpert.*”, International Conference on Parallel and Distributed Processing Techniques and Applications, July 2011.
- ▶ **A. Rane** and D. Stanzone, “*Experiences in Tuning Performance of Hybrid MPI/OpenMP applications on Quad-core Systems*”. LCI International Conference on High-Performance Clustered Computing, 2009.

## Professional Activities

- ▶ **Student Program Committee member** for IEEE Security and Privacy (*Oakland*) conference, 2017 and for International Conference on Architectural Support for Programming Languages and Operating Systems (ASPLOS) 2018.
- ▶ **SxSW Edu Panel Member** for discussion on research opportunities for undergraduate students, 2016.
- ▶ **Reviewer** for International Summer School on HPC Challenges in Computational Sciences, 2012 and 2013.
- ▶ **M.S. Selection Committee Member** for the Computer Science department at The University of Texas at Austin, 2013.

## Media Coverage

- ▶ Podcast interview by The Daily Texan on my freshman course on security.  
<https://soundcloud.com/thedailytexan/longhorn-lab-report-march-24th-2016>
- ▶ Editorial in the Austin American-Statesman about my freshman course.  
<https://www.statesman.com/NEWS/20160924/Small-cities-must-block-cyberhacks>
- ▶ College of Natural Sciences article on my freshman course.  
<https://cns.utexas.edu/news/freshmen-fight-cyber-attacks>
- ▶ Podcast on my research on the PerfExpert performance diagnosis tool.  
<https://www.rce-cast.com/Podcast/rce-77-perfexpert.html>