Ashay Rane

Contact Information
GDC 5.518F, 1 University Station, ashay.rane@utexas.edu
Stop C0500, Austin, TX - 78712 https://ashay.rane.info

Research Interests
Secure Systems, Compilers, Computer Architecture, and Program Verification

Education

- **PhD in Computer Science** GPA: 3.54
  The University of Texas at Austin, Austin, Texas Aug 2012 — present
- **Master of Science in Computer Science** GPA: 4.00
  Arizona State University, Tempe, Arizona Aug 2007 — Nov 2007
- **Bachelor of Engineering in Computer Engineering** Aggregate: 72.43%
  Mumbai University, Mumbai, India Jun 2003 — Jul 2006

Honors and Awards

- **Distinguished Paper Award**, at the 26*th* USENIX Security Symposium (2017).
- **Brumley Senior Next-Generation Fellow**, Robert Strauss Center for International Security and Law, The University of Texas at Austin (2015 and 2016).
- **Best Paper Nominee**, at the 21*st* International Conference on Parallel Architectures and Compilation Techniques (2012).

Recent Work Experience

- **Graduate Research Assistant, Computer Science, UT Austin** Jan 2017 — present
  I do research in compiler and microarchitectural defenses against side-channel attacks.
- **Research Educator (Instructor), UT Austin** Jan 2015 — Dec 2016
  I taught a freshman course on computer security [`https://cs.utexas.edu/users/fri-security`], where the objective was to teach research skills to freshman students. Students critiqued research papers, discussed extensions, and implemented research projects.
- **Intern, Microsoft Research, Redmond, Washington** May 2016 — Aug 2016
  As part of the Project Everest group [`https://project-everest.github.io`], I designed and implemented the verification of the absence of digital side channels using the Dafny verifier.
- **Intern, Google, Mountain View, California** May 2013 — Aug 2013
  I analyzed and optimized the performance of Cloud SQL on Google's infrastructure.
- **Research Associate, Texas Advanced Computing Center** Dec 2010 — Aug 2012
  Graduate Research Assistant, Computer Science, UT Austin Sep 2012 — Dec 2014
  I researched and developed tools for performance diagnosis of data center applications.

Ashay Rane

Publications

- B. Bond, C. Hawblitzel, M. Kapritsos, K. Leino, J. Lorch, B. Parno, **A. Rane**, S. Setty, L. Thompson, *"Vale: Verifying High-Performance Cryptographic Assembly Code"*, USENIX Security, Symposium, August 2017. **Distinguished Paper Award**

- **A. Rane**, C. Lin, M. Tiwari, *"Secure, Precise, and Fast Floating-Point Operations on x86 Processors"*, USENIX Security Symposium, August 2016.

- **A. Rane**, C. Lin, M. Tiwari, *"Raccoon: Closing Digital Side-Channels through Obfuscated Execution"*, USENIX Security Symposium, August 2015.

- **A. Rane**, R. Krishnaiyer, C. Newburn, J. Browne, L. Fialho, Z. Matveev, *"Unification of Static and Dynamic Analyses to Enable Vectorization"*, International Workshop on Languages and Compilers for Parallel Computing (LCPC), September 2014.

- **A. Rane**, J. Browne, *"Enhancing performance optimization of multicore/multichip nodes with data structure metrics"*, ACM Transactions on Parallel Computing, May 2014.

- **A. Rane**, J. Browne, *"Enhancing performance optimization of multicore chips and multichip nodes with data structure metrics"*, Parallel Architectures and Compilation Techniques (PACT), September 2012 - Nominated as one of 3 best papers of the conference.

- **A. Rane**, J. Browne, L. Koesterke, *"A Systematic Process for Efficient Execution on Intel's Heterogeneous Computation Nodes"*, Extreme Science and Discovery Environment (XSEDE), July 2012.

- **A. Rane**, J. Browne, L. Koesterke, *"PerfExpert and MACPO: Which code segments should (not) be ported to MIC? "*, TACC-Intel Highly Parallel Computing Symposium, April 2012.

- **A. Rane**, S. Sardeshpande, J. Browne, *"Determining code segments that can benefit from execution on GPUs."*, Supercomputing Conference (SC) 2011, November 2011.

- **A. Rane**, J. Browne, *"Performance Optimization of Data Structures using Memory Access Characterization"*, IEEE International Conference on Cluster Computing (CLUSTER), 2011, September 2011.

- O. A. Sopeju, M. Burtscher, **A. Rane**, and J. Browne, *"AutoSCOPE: Automatic Suggestions for Code Optimizations Using PerfExpert"*, International Conference on Parallel and Distributed Processing Techniques and Applications, July 2011.

- **A. Rane** and D. Stanzione, *"Experiences in Tuning Performance of Hybrid MPI/OpenMP applications on Quad-core System"*, LCI International Conference on High-Performance Clustered Computing, 2009.

Ashay Rane

Professional Activities

- **Student Program Committee Member** for IEEE Security and Privacy (Oakland) conference, 2017.
- **SxSWEdu Panel Member** for discussion on research opportunities for undergraduate students, 2016.
- **Reviewer** for International Summer School on HPC Challenges in Computational Sciences, 2012 and 2013.

Media Coverage

- Podcast interview by The Daily Texan on my freshman course on security.
  `https://goo.gl/G97NqZ`
- Editorial in the Austin American-Statesman about my freshman course.
  `https://goo.gl/8kAcNV`
- College of Natural Sciences article on my freshman course.
  `https://goo.gl/Ru7aS6`
- Podcast on my research on the PerfExpert performance diagnosis tool.
  `https://goo.gl/ZbKlwD`